WHAT IS CLAIMED IS:

1. A simulator is comprising:

a simulation CPU;

a memory write-accessible from one of said simulation CPU and a control CPU connected to said simulator and read-accessible from the other;

means for causing said simulation CPU to read out control information written in said memory by the control CPU; and

means for writing an execution result of execution of simulation based on the control information in said memory in a state readable by the control CPU.

2. A simulator according to claim 1, wherein

said simulator further comprises connection means for connecting said simulation CPU to said memory, and

the control information is read out from said memory or the execution result is written in said memory through said connection means.

3. A simulator according to claim 1, wherein after the execution result of the simulation is written in said memory, an interrupt is requested of the control CPU.

4. A simulator according to claim 3, further comprising

count means for counting the interrupt, and

transmission means for transmitting timeout data on the basis of a count value of said count means.

5. A simulator comprising:

a first memory in which control information is written by a control CPU connected to said simulator;

a second memory from which information can be read out by the control CPU;

means for reading out the control information from said first memory;

means for generating information of a control result based on the readout control information; and

means for writing the generated information of the control result in said second memory.

6. A simulator according to claim 5, wherein after the information of the control result is written in said second memory, an interrupt is requested of the control CPU.

7. A simulator according to claim 6, further comprising

count means for counting the interrupt, and

transmission means for transmitting timeout data on the basis of a count value of said count means.

8. A simulator according to claim 5, wherein the control information corresponds to a command, and the control result corresponds to a response.

9. A simulator comprising:

a first memory from which information can be read out by a control CPU connected to said simulator; and

means for periodically writing a sensor status in

said first memory.

10. A simulator according to claim 9, further comprising

a second memory in which a command is written by the control CPU,

means for reading out the command from said second memory,

means for generating a response based on the readout command, and

means for writing the generated response in said first memory.

11. A simulator according to claim 10, further comprising

a third memory in which output port ON/OFF information is written by the control CPU, and

means for reading out the output port ON/OFF information from said third memory.

12. A simulator according to claim 9, wherein after the sensor status is written in said first memory, an interrupt is requested of the control CPU.

13. A simulator according to claim 12, further comprising

count means for counting the interrupt, and

transmission means for transmitting timeout data on the basis of a count value of said count means.

14. A simulation method comprising the steps of:

causing a control CPU to write control information

in a first memory;

causing a simulation CPU to read out the control information written in the first memory;

causing the simulation CPU to execute simulation based on the control information;

causing the simulation CPU to write a simulation result in a second memory; and

causing the control CPU to read out the simulation result written in the second memory.

15. A method according to claim 14, further comprising the step of, after the simulation result is written in the second memory, requesting an interrupt of the control CPU.

16. A method according to claim 15, further comprising the steps of

counting the interrupt, and

transmitting timeout data on the basis of a count value of the interrupt.

17. A simulator for simulating operation on a unit side in an apparatus which transmits command information from a main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, comprising:

a command memory for holding the command information transmitted from the main body side, said command

memory being read-accessible from a unit-side CPU;

a sensor memory in which the sensor information can be written by the unit-side CPU;

means for transmitting the sensor information written in said sensor memory to the main body side;

a response memory in which response information can be written by the unit-side CPU; and

means for transmitting the response information written in said response memory to the main body side.

18. A simulator according to claim 17, wherein

said simulator further comprises

an address memory for holding a self address in advance, and

comparison means for comparing the self address held in said address memory with a designated address designated on the main body side, and

when a comparison result by said comparison means indicates that the addresses match, the sensor information is received, the command information is received, and the response is sent.

19. A simulation system comprising:

a first simulator and a second simulator, each being connected to a main body, for simulating operation on a unit side,

said first simulator comprising means for receiving sensor information transmitted from said second simulator to said main body side, and

said first simulator operating in synchronism with said second simulator on the basis of the received sensor information.

20. A system according to claim 19, wherein said system simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, and

said first simulator comprises

a command memory for holding the command information transmitted from the main body side, said command memory being read-accessible from a unit-side CPU;

a sensor memory in which the sensor information can be written by the unit-side CPU;

means for transmitting the sensor information written in said sensor memory to the main body side;

a response memory in which response information can be written by the unit-side CPU; and

means for transmitting the response information written in said response memory to the main body side.

21. A system according to claim 20, wherein said first simulator comprises a port memory for holding port information transmitted from the main body side, said port memory being read-accessible from the

unit-side CPU.

22. A simulator for simulating operation on a unit side in an apparatus which transmits command information from a main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, comprising:

a first command memory for holding command information transmitted from said main body side via a first series, said first command memory being read-accessible from a unit-side CPU;

a sensor memory in which the sensor information can be written by the unit-side CPU;

means for transmitting the sensor information written in said sensor memory to said main body side via said first series;

a response memory in which response information can be written by the unit-side CPU;

means for transmitting the response information written in said response memory to the main body side via said first series; and

a second command memory for holding command information transmitted from said main body side via a second series, said second command memory being read-accessible from the unit-side CPU.

23. A simulation system comprising:

a first simulator and a second simulator,

said first simulator comprising means for receiving sensor information transmitted from said second simulator to said main body side via a second series,

said first simulator operating in synchronism with said second simulator on the basis of the received sensor information,

said second simulator comprising means for receiving sensor information transmitted from said first simulator to said main body side via a first series, and

said second simulator operating in synchronism with said first simulator on the basis of the received sensor information.

24. A system according to claim 23, wherein

said system simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, and

said first simulator comprises

a first command memory for holding command information transmitted from said main body side via said first series, said first command memory being

read-accessible from a unit-side CPU;

a sensor memory in which the sensor information can be written by the unit-side CPU;

means for transmitting the sensor information written in said sensor memory to said main body side via said first series;

a response memory in which response information can be written by the unit-side CPU;

means for transmitting the response information written in said response memory to said main body side via said first series; and

a second command memory for holding command information transmitted from said second main body side via said second series, said second command memory being read-accessible from the unit-side CPU.

25. A system according to claim 24, wherein said first simulator comprises

a port memory for holding port information transmitted from said main body side via said first series, said port memory being read-accessible from the unit-side CPU, and

a port memory for holding port information transmitted from said main body side via said second series, said port memory being read-accessible from the unit-side CPU.

26. A simulation method of simulating operation on a unit side in an apparatus which transmits command

information from a main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, comprising the steps of:

holding the command information transmitted from the main body side in a state read-accessible from a unit-side CPU; and

transmitting sensor information and response information written by the unit-side CPU to the main body side.

27. A simulation method applied to a simulation system including first and second simulators, comprising the steps of:

causing the first simulator to receive sensor information transmitted from the second simulator to a main body side; and

causing the first simulator to operate in synchronism with the second simulator on the basis of the received sensor information.

28. A method according to claim 27, wherein

said method simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the

unit side to the main body side, and

said method further comprises the steps of

causing the first simulator to hold the command information transmitted from the main body side in a state read-accessible from a unit-side CPU, and

causing the first simulator to transmit the sensor information and response information written by the unit-side CPU to the main body side.

29. A simulation method of simulating operation on a unit side in an apparatus which transmits command information from a main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, comprising the steps of:

holding command information transmitted from said main body side via a first series and command information transmitted from said main body side via a second series in a state read-accessible from a unit-side CPU; and

transmitting sensor information and response information written by the unit-side CPU to said main body side via said first series.

30. A simulation method applied to a simulation system including first and second simulators and a main body, comprising the steps of:

causing the first simulator to receive sensor

information transmitted from the second simulator to said main body side via a second series;

causing the first simulator to operate in synchronism with the second simulator on the basis of the received sensor information;

causing the second simulator to receive sensor information transmitted from the first simulator to said main body side via a first series; and

causing the second simulator to operate in synchronism with the first simulator on the basis of the received sensor information.

31. A method according to claim 30, wherein

said method simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, and

said method further comprises the steps of

causing the first simulator to hold command information transmitted from said main body side via a first series and command information transmitted from said main body side via a second series in a state read-accessible from a unit-side CPU, and

causing the first simulator to transmit the sensor information and response information written by the

unit-side CPU to said main body side via a fist series.